Listing and Amendments to the Claims

This listing of claims will replace all previous versions and listings of claims:

1.(currently amended) An active matrix electroluminescent display device comprising an array of display pixels ~~(1)~~, each pixel comprising:

an electroluminescent (EL) display element ~~(2)~~;

a drive transistor ~~(22)~~ for driving a current through the display element, a drive voltage being provided to the gate of the drive transistor ~~(22)~~; and

a storage capacitor ~~(30)~~ for storing a drive level, said storage capacitor ~~and~~ connected between an input ~~(6)~~ to the pixel and the gate of the drive transistor ~~(22)~~,

wherein driver circuitry ~~is provided for providing~~ provides a stepped voltage waveform to the input ~~(6)~~ of the pixel, the stepped voltage waveform being voltage-shifted by the storage capacitor ~~(30)~~ before application to the gate of the drive transistor ~~(22)~~, and wherein the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor ~~(22)~~.

2.(previously presented) A device as claimed in claim 1, wherein the height of the steps in the stepped voltage waveform is sufficient to include the linear operating region voltages of the drive transistors of all pixels of the display.

3.(currently amended) A device as claimed in claim 1 ~~or 2~~, wherein the drive level is selected to have one of a plurality of values, and is selected such that any gate voltage for the drive transistor in the linear region corresponds to a voltage between steps of the voltage applied to the gate of the drive transistor.

4.(currently amended) A device as claimed in ~~any preceding~~ claim 1, wherein each pixel further comprises an address transistor ~~(32)~~, connected between a power supply line ~~(26)~~ and the gate of the drive transistor ~~(22)~~.

5.(currently amended) A device as claimed in claim 4, wherein each pixel further comprises means for disabling the driving of current by the drive transistor ~~(22)~~ through the display element ~~(2)~~.

6.(currently amended) A device as claimed in claim 5, wherein the means for disabling comprises an isolating transistor ~~(34)~~ in series with the drive transistor ~~(22)~~ and the display element ~~(2)~~.

7.(currently amended) A device as claimed in claim 4, wherein the device further comprises disabling means comprising a switch for switching the voltage on one terminal of the display elements ~~(2)~~ of the array of pixels.

8.(currently amended) A device as claimed in claim 5~~, 6 or 7~~, wherein the device is operable in two modes:

a first mode in which a pixel voltage ~~(42a)~~ is applied to the input ~~(6)~~ to the pixel, the address transistor ~~(32)~~ is turned on, the disabling means is turned on to turn off the display element ~~(2)~~ and the storage capacitor ~~(30)~~ is charged to a level derived from the drive voltage ~~(42a)~~; and

a second mode in which the address transistor ~~(32)~~ is turned off, the disabling means is turned off and the stepped voltage waveform ~~(42b)~~ is applied to the input ~~(6)~~ of the pixel.

9.(currently amended) A device as claimed in ~~any preceding~~ claim 1, wherein the device is operable in at least two sequential phases, one phase ~~(60)~~ providing coarse resolution pulse width modulation and the other, shorter phase ~~(62)~~, providing fine resolution pulse width modulation.

10.(currently amended) A method of addressing an active matrix electroluminescent display device comprising an array of display pixels ~~(1)~~, each pixel comprising an electroluminescent (EL) display element ~~(2)~~, a drive transistor ~~(22)~~ for driving a current through the display element ~~(2), a drive voltage being provided to the gate of the drive transistor (22)~~, and a storage capacitor ~~(30) for storing a drive level and~~ connected between an input ~~(6)~~ to the pixel and the gate of the drive transistor ~~(22)~~, the method comprising~~, for each pixel~~:

storing a ~~pixel~~ drive ~~voltage~~level ~~(46)~~ on the storage capacitor ~~(30)~~;

providing a stepped voltage waveform ~~(42b)~~ to the input of the pixel ~~(6)~~, the stepped voltage waveform being voltage-shifted by the storage capacitor before application to ~~the~~ a gate of the drive transistor, such that for a first set of the voltage steps applied to the gate of the drive transistor, the drive transistor is turned on, and for a second set of the voltage steps applied to the gate of the drive transistor, the drive transistor is turned off, the first and second sets being determined by the stored ~~pixel~~ drive level ~~(46)~~.

11.(previously presented) A method as claimed in claim 10, wherein the height of the steps in the stepped voltage waveform is greater than the voltage width of the linear operating region of the drive transistor.

12.(previously presented) A method as claimed in claim 11, wherein the height of the steps in the stepped voltage waveform is greater than the voltage width of the overlaid linear operating region voltages of the drive transistors of all pixels of the display.

13.(currently amended) A method as claimed in ~~any one of claims~~ claim 10 ~~to 12~~, wherein the drive level is selected to have one of a plurality of values, and is selected such that any gate voltage for the drive transistor in the linear region corresponds to a voltage between steps of the voltage applied to the gate of the drive transistor.

14.(currently amended) A method as claimed in ~~any one of claims~~ claim 10 ~~to 13~~, wherein the step of storing a pixel drive level ~~(46)~~ on the storage capacitor comprises turning on an address transistor ~~(32)~~ connected between a power supply line ~~(26)~~ and the gate of the drive transistor ~~(22)~~ and charging the storage capacitor ~~(30)~~ using the address transistor.

15.(previously presented) A method as claimed in claim 14, further comprising disabling the driving of current by the drive transistor through the display element during the storing of a pixel drive level on the storage capacitor.

16.(currently amended) A method as claimed in ~~any one of claims~~claim 10 ~~to 15~~, wherein the device is operable in at least two sequential phases, one phase ~~(60)~~ providing coarse resolution pulse width modulation and the other, shorter phase ~~(62)~~, providing fine resolution pulse width modulation.

17.(currently amended) A method as claimed in claim 16, wherein the stepped voltage waveform to the input of the pixel has the same voltage levels in the two phases ~~(60, 62)~~, and the shorter phase has shorter step transitions.